A New High Speed 16x16 Vedic Multiplier

Shauvik Panda, Dr. Alpana Agarwal

Abstract— In this paper, a novel architecture of Vedic multiplier with 'Urdhava-Tiryakbhyam' methodology for 16 bit multiplier and multiplicand is proposed with the use of three adders namely modified Kogge-Stone Adder, Carry Select Adder and Compressor Adders. They are chosen as they decrease vertical critical delay in comparison to the conventional architectures of Vedic Multipliers and thus help to improve the speed of Multiplication process. The design is coded in Verilog HDL and is implemented using Xilinx ISE 14.5. The delay calculated for the proposed multiplier is 11.511ns and it is further compared to conventional multipliers.

Index Terms—Vedic multiplication, Compressor adder, Kogge Stone Adder, Urdhava-Tiryakbhyam,

1 Introduction

We all use smart phones that are inbuilt with latest features but sometimes we face situation where our phone gets hang or display message like system not responding the reasons behind it is the speed of the processor and the speed of the processor merely depends on how fast it is performing the multiplications as all data processing involve multiplication so multiplication is the building block operation that describes the speed. In recent years speed, power and area is the main concern in VLSI domain. Vedic multiplier is built on Vedic mathematics which further is extracted from the ancient Vedas by the Sri Bharati Krishna Tirthaji in between 1911 and 1918. The specialty of Vedic mathematics is that it gives simple way to solve the calculations which can be easily understood by human minds. This Vedic mathematics is divided into 16 sutras which give different rules for the simplification of the problems related to trigonometry, algebra, geometry etc. The Urdhva-Triyakbhyam sutra used in this paper is derived from ancient Vedas and this sutra is a universal method of multiplication [3]. The method has been explained below in Fig 1.

Pushpalata [7] proposed architecture with the ripple carry adder in Vedic multiplication unit for 4 bit binary numbers. This architecture can be extended for higher bits like 8, 16, 32 bit multiplications. Later, a Fast and low power 16-bit multiplier architecture was proposed by R.K, R.S, S. Sarkar, and Rajesh [8] replacing ripple carry adder with the carry lookahead adder. The power dissipated and propagation delay time is 0.17 mW and 27.15 ns respectively. But the device utilization of the architecture was very high. Devika, Kabiraj and Rutuparna [9] proposed an alternate architecture for 8 and 16-bit multiplication using carry save adders. This further increased the speed performance of the multiplier and had a combinational delay of 18.58 ns. A tree multiplication design for Vedic multiplier had been proposed by Abhishek, Utsav and Vinod [10], which uses a new addition tree structure for the addition of partially generated products which is built on decimal arithmetic multiplication principle for three digit length of multiplier and multiplicand. This design had a delay of 15.718 for 16 bit multiplication.

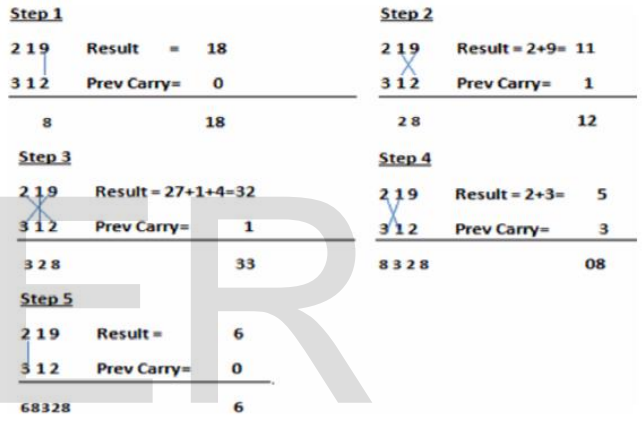

Fig. 1. Urdhva-Triyakbhyam sutra for decimal numbers.

In this paper we have proposed a modified Vedic multiplier that has less delay compared to conventional Vedic Multipliers. Compressor adders have been used over conventional architectures of half-adders and full adders because of their higher speed performance. These compressors actually act as counters and count the number of 1s in the given bits and thus behave as adders. They make use of multiplexer in addition with half-adders and full adders which allow the use of lesser XOR gates. The rest of paper is organized as follows. Section 2 presents the Urdhva-Triyakbhyam sutra used in Vedic Multiplier. Section 3 presents the implementation of the multiplier on FPGA. Section 4 provides the experimental results of our design. In Section 5 we conclude this work.

2 Vertically and Crosswise Technique

The Sanskrit name for this rule is 'Urdhva-Triyakbhyam' which is a universal formula for the multiplication [1]. This method multiplies the digits vertically and crosswise and finally adds them with the help of the appropriate adder. This rule is applicable to both integers and binary numbers. The best feature of this method is that the partial products needed for the multiplication are already generated in advance and this leads to decrease in delay and thus saves the time. The

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increase in number of bits however brings little increase in area and critical delay. The method is explained for multiplication of decimal numbers and binary numbers differently.

2.1 For Decimal Number

For N digit number there will be 2N−1 steps. The digits on the ends of the line are multiplied and result is stored. Then the previous carry is added to it. The least significant digit of resultant coming from addition is kept as answer bit of the multiplication and all other digits are considered as previous carries for the next step. When the number of lines becomes more than one in the same step, then all the outcomes are accumulated with the previous carries. Following same steps, final output of multiplication comes. Initial carry in this case is taken as zero. Fig. 1 shows the multiplication of two 3 digit decimal numbers, 325 and 738 in five steps.

2.2 For Binary Numbers

The same way is extended to the binary digit multiplication. One bit multiplication is simple AND gate operation of the operands. For the higher bit product, the following method is used for the evaluation of the equations for the resultant bits of multiplication. This method is known as square table method. In this technique firstly each small square block inside the table is partitioned into two identical parts. Then multiplier and multiplicand are written on the successive sides of the table. After that each bit of them is multiplied separately and result is stored in the lower part of small square block. Then starting from least significant bit of multiplier, all the bits coming in lower part of small square blocks are added and sum bit of the their resultant is considered as the resultant bit of the multiplication. Carry bits of the addition are further sent to succeeding blocks and also added to the results coming in their way. Fig. 2 shows the multiplication of the two binary numbers a=a3a2a1a0(4 bits) and b=b3b2b1b0(4 bits) and final product is r7r6r5r4r3r2r1r0(8 bit). Because partial products are generated in parallel, so the critical delay will be only the time taken by the signal to pass through the logical gates.

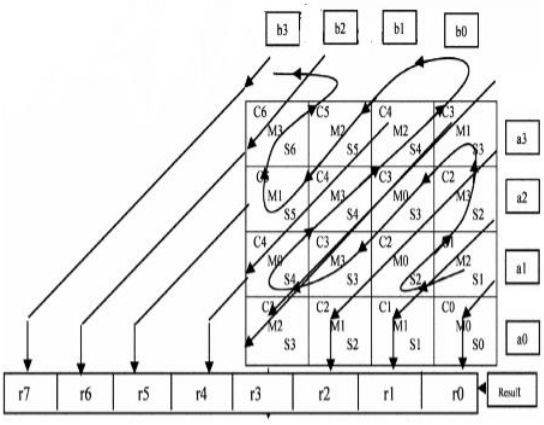

Fig.2 4x4 binary Vedic multiplication.

3 Implementation of Proposed Design

The conventional Vedic multiplier uses Ripple Carry Adders [4]. The Ripple Carry Adder has limitations in terms of time it takes to propagate the carry. On comparison of other adders, we see that Kogge-Stone Adder is the fastest adder but it requires lot of area which increases with number of bits. In order to reduce the area of the Kogge-Stone adder, we propose a modified architecture which reduces the area of adder as well as the delay of Adder. Fig.3 shows a comparison of the conventional architecture of the Kogge-Stone Adder and the modified architecture of Kogge-Stone Adder.

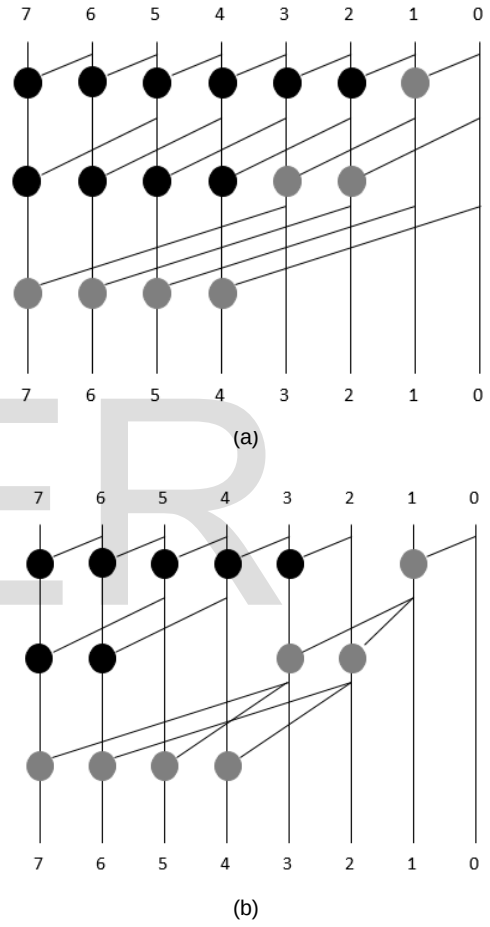

Fig.3 (a) Conventional Kogge-Stone Adder, (b) Modified Kogge-Stone Adder.

All the nodes in the architecture denotes a carry operator which includes generate and propagate function as shown in Fig.4. The grey nodes represent the carry nodes that are necessary for result in final stage. The black nodes represent the intermediate carry function. We can change the properties of the adder by changing the routing and eliminating the black nodes in a conventional architecture. But all these changes do not yield favorable results. Since our focus is on increasing the speed, we eliminate 3 black nodes, corresponding to bits 4 and 5 in second stage and bit 2 in first stage. We then reroute the design to provide the correct results. The elimination of the redundant nodes help to reduce the area and increase speed of

the design.

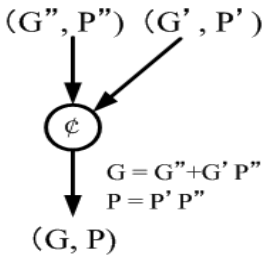

Fig.4 Carry Operator Function.

Compressor Adders [6] and Carry Select Adders also have comparable speeds for bit lengths up to 16 with slightly lower area utilization. Thus in this design, in order to obtain high speed, without considerable increase in area, we have used a combination of all three adders to design the Vedic Multiplier. The architecture of a 3 bit compressor adder is shown in Fig.5.

Initially a 2x2 Vedic multiplier is designed using full adder and half adder. The 4x4 multiplier is then built using four 2x2 multipliers, two 6 bit compressor adders and one modified 4 bit Kogge-Stone adder. Fig.6 shows the architecture of the 4x4 multiplier.

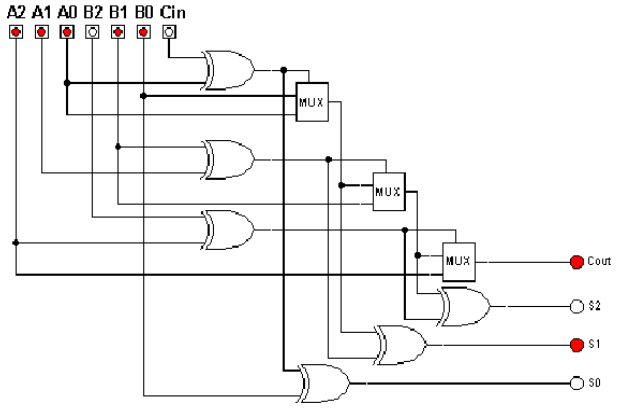

Fig.5 3 bit compressor adder.

The 8x8 Vedic multiplier is then build using the 4x4 multiplier, two 12 bit compressor adders and one 8 bit Carry select adder. The 16x16 multiplier is designed using four 8x8 multipliers, two 24 bit modified Kogge-Stone Adder and one 16 bit Carry Select Adder. Fig.7 shows the architecture of the modified 16x16 Vedic multiplier.

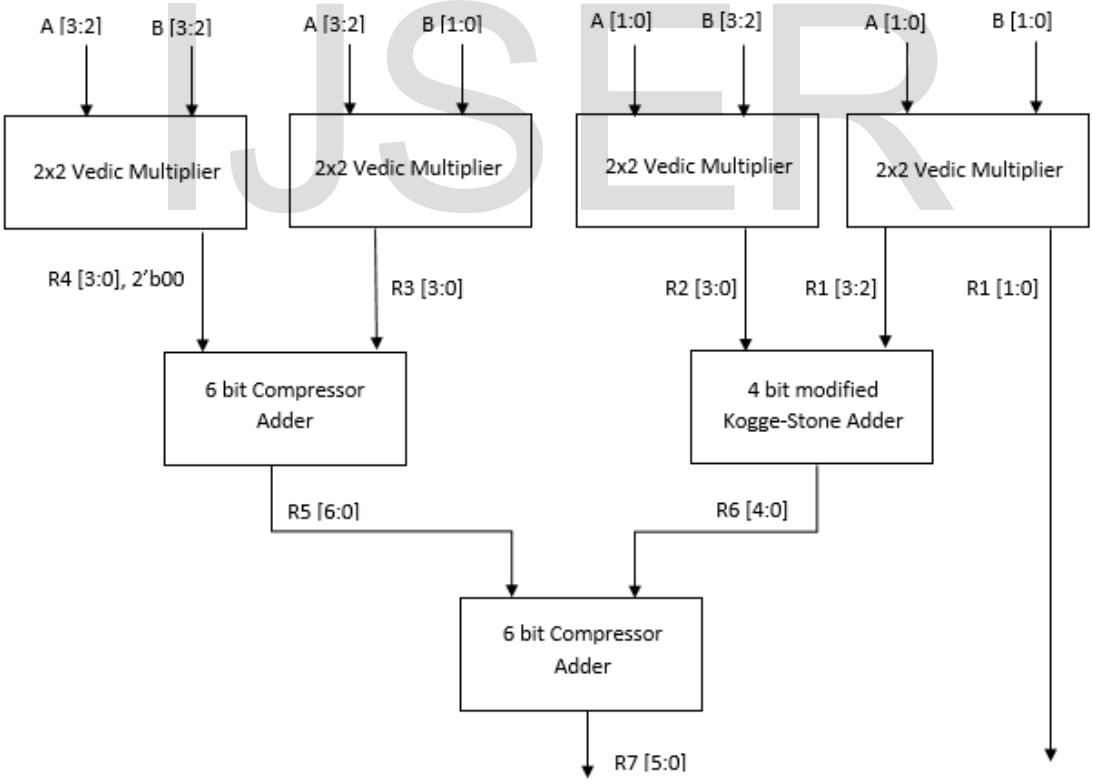

Fig.6 Architecture of modified 4x4 Vedic Multiplier.

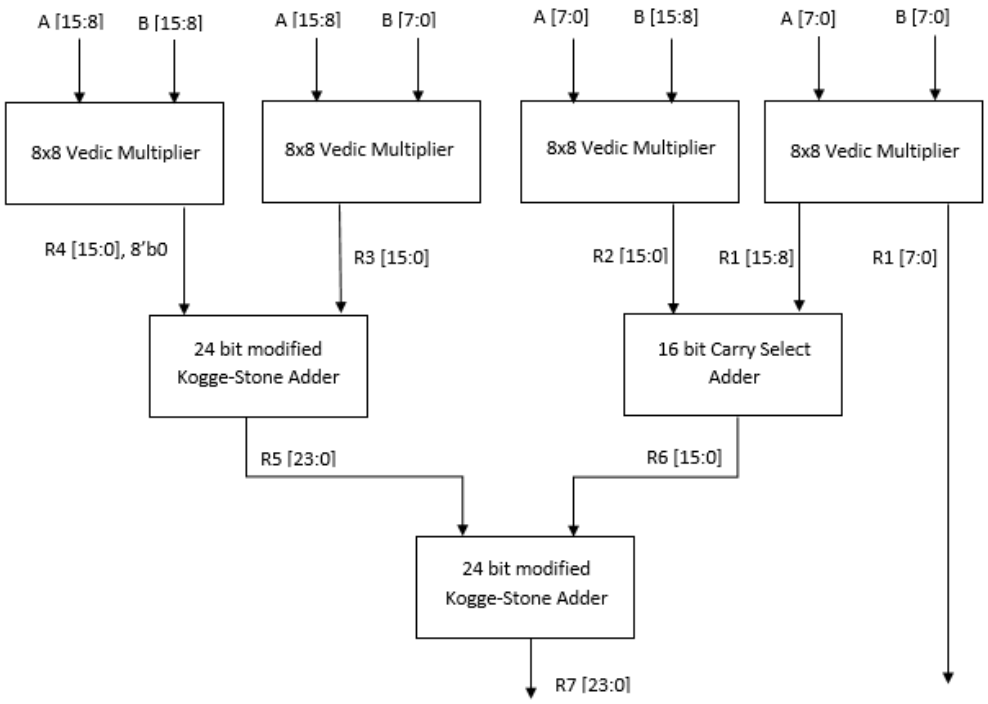

Fig.7 Architecture of modified 16x16 Vedic Multiplier.

4 Results and Comparison

The RTL schematic of the base Vedic multiplier is shown in Fig.8 and the RTL of proposed Vedic Multiplier is shown in Fig 9. As mentioned earlier we see that the 16x16 Vedic Multiplier uses two 24 bit compressor adder and one 16 bit Carry Select adder.

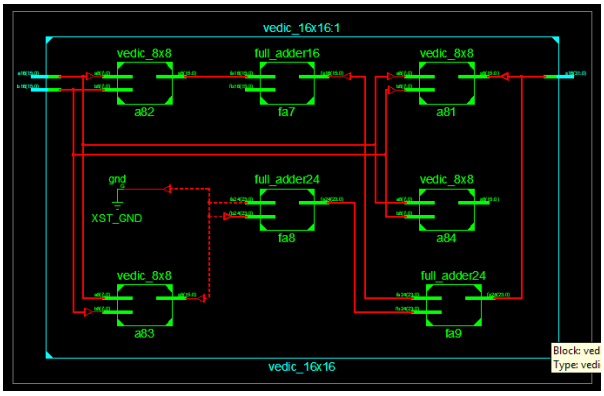

Fig.8 RTL schematic of Base 16x16 Vedic Multiplier.

The simulation results of the modified 16x16 Vedic multiplier is shown in Fig.10. A comparison of delay of the modified Vedic multiplier with basic Vedic Multiplier and other conventional adders is made in Table 1. The entire design is implemented using Xilinx ISE 14.5 using Verilog HDL.

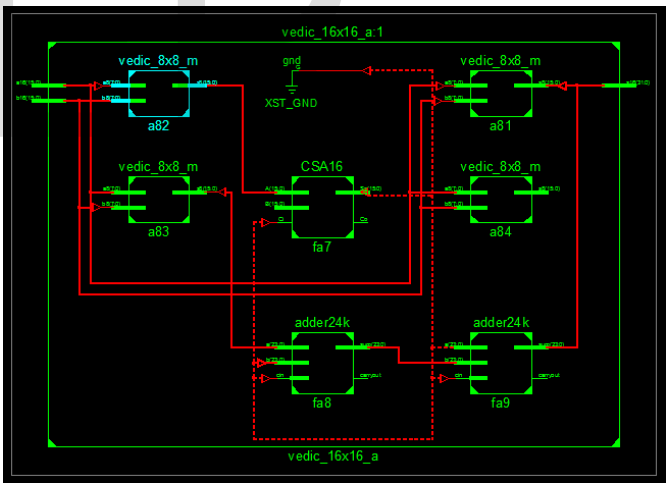

Fig.9 RTL schematic of 16x16 Proposed Vedic Multiplier.

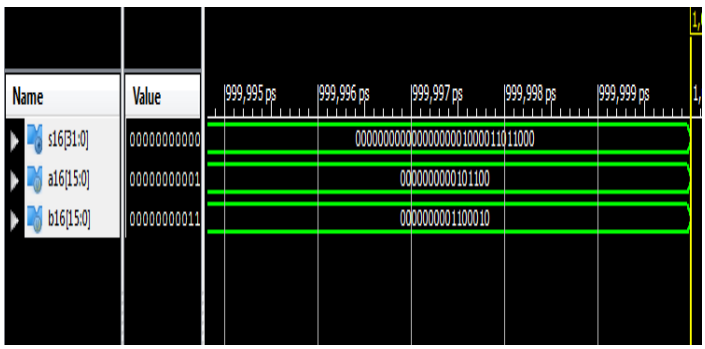

Fig.10 Simulation Result of 16x16 Vedic Multiplier.

Table 1 Comparison of Proposed multiplier with previous multipliers.

16 bit Multiplier	Delay(ns)	% Improvement
Array Multiplier [2]	43.946	73.8
Wallace Tree Multiplier [2]	46.046	75
Booth Multiplier [2]	37.041	68.9
Base Vedic Multipliers	16.180	27.74
Proposed Vedic Multiplier	11.511	

5 Conclusion

In this paper, a modified Vedic Multiplier is proposed that uses a combination of three different type of adders. The use of compressors adders and Modified Kogge Stone Adder greatly reduces the delay of the design. It also reduces the stage operation simultaneously. It can be used where stringent demands of speed are required. It can be a great use in digital signal processing applications. As the parallel generation of partial products are generated and unwanted multiplication steps has been removed so speed increases which was the main concern.

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